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Guest Editorial

## Advances in Wafer Level Packaging (WLP)

Wafer level packages (WLPs) with various design configurations are rapidly gaining tremendous applications throughout semiconductor industry due to small-form factor, low-cost, and high performance. Because of the innovative production processes utilized in WLP manufacturing and the accompanying rise in the price of gold, the traditional wire bonding packages are no longer as attractive as they used to be. In addition, WLPs provide the smallest form factor to satisfy multifunctional device requirements along with improved signal integrity for today's handheld electronics. Existing wire bonding devices can be easily converted to WLPs by adding a redistribution layer (RDL) during backend wafer level processing. Since the input/output (I/O) pads do not have to be routed to the perimeter of the die, the WLP die can be designed to have a much smaller footprint as compared to its wire bonding counterpart, which means more area-array dies can be packed onto a single wafer to reduce overall processing costs per die. Conventional (fan-in) WLPs are formed on the dies while they are still on the uncut wafer. The result is that the final packaged product is the same size as the die itself. Recently, fan-out WLPs have emerged. Fan-out WLP starts with the reconstitution or reconfiguration of individual dies to an artificial molded wafer. Fan-out WLPs eliminate the need of expensive substrate as in flip-chip packages, while expanding the WLP size with molding compound for higher I/O applications without compromising on the board level reliability. Essentially, WLP enables the next generation of portable electronics at a competitive price. Many future products using through-silicon-via (TSV) technology will be packaged as WLPs.

There have been relatively few publications focused on the latest results of WLP development and research. Many design guidelines, such as material selection and geometry dimensions of under bump metallurgy (UBM), RDL, passivation and solder alloy, for optimum board level reliability performance of WLPs, are still based on technical know-how gained from flip-chip or wire bonding BGA reliability studies published in the past two decades. However, WLPs have their unique product requirements for design guidelines, process conditions, material selection, reliability tests, and failure analysis. In addition, WLP is also an enabling technology for 3D package and system-in-package (SIP), justifying significant research attention.

The timing is therefore ripe for this edition to summarize the state-of-the-art research advances in wafer level packaging in various fields of interest. Integration of WLP in 3D packages with TSV or wireless proximity communication (PxC), as well as applications in Microelectromechanical Systems (MEMS) packaging and power packaging, will be highlighted in this issue. In addition, the state-of-the-art simulation is applied to design for enhanced package and board level reliability of WLPs, including thermal cycling test, drop test, electromigration test, probe test, etc. Besides, research work in the area of solder joint and impact characterization of WLPs, critical for portable electronics applications, will be shared. In this special issue on *advances in wafer level packaging (WLP)*, we have collected 12 papers written by the experts in the field, reviewing and demonstrating the latest research and development in WLP.

The first paper by Ko and Chen reviews recent research efforts in wafer-level bonding technologies, including bonding materials and bonding conditions. The corresponding 3D integration technologies and platforms are described and discussed. Shen et al. share the considerations in developing an advanced clamped through-silicon-via (C-TSV) interconnection technology for 3D chip-to-chip or chip-to-wafer packaging. On the other hand, Sze et al. demonstrate active monitoring of chip-to-chip alignment during thermal cycling of a PxC enabled package that facilitates the integration of VLSI chips in a package using near-field capacitive coupling between chips, eliminating the need for solder or wires for I/O at the chip-to-chip interface. In the 4th paper by Jang et al., an advanced regression scheme is proposed to analyze fine leak batch testing data of wafer-level hermetic MEMS packages. In a review paper by Liu, the details on how advances in both semiconductor content and power advanced wafer level package design and materials have co-enabled significant advances in power device capability during recent years are covered. In another work, Chen et al. study the interplay between structural design, process interactions, and present possible solutions for RDL in high power WLPs.

The 7th paper by Hochstenbach et al. features major research and development results on understanding and enhancing the first and second level reliability of WLPs using combined experimental and virtual prototyping (thermal, mechanical and thermo-mechanical) techniques. From a structural design point of view, Fan et al. investigate solder joint thermo-mechanical reliability performance of a variety of fan-in and fan-out WLPs. Thermo-mechanical reliability of conventional fan-in WLPs including ball on I/O, ball on polymer with or without UBM, and copper post WLPs, and the emerging fan-out WLPs such as embedded wafer level ball grid array (eWLB) packages and redistributed chip scale packages (RCP), are discussed. In a research to improve the electromigration performance of solder joints in an encapsulated copper post WLP, Dandu et al. propose two new line-to-bump geometry designs. In the 10th paper, Chang et al. examine probe card with ultra-long probing needles for digital light processing (DLP) wafer testing, presenting a compromised design that considers minimizing scrub length and buckling potential conjointly. For material research, Su et al. characterize the shear and pull strengths of lead-free solder joint array of WLP with Ti/Cu/Ni/Au UBM. In the last paper by Crosbie and Lee, a series of dynamic four-point bend tests were conducted to evaluate the multiple impact reliability of WLP samples, aiming to better understand the failure modes and

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actual reliability of WLP under uniaxial loading, which is commonly observed in drop simulations and tests of mobile devices.

We are grateful to the participating authors and reviewers, who have devoted to the subject and altogether contributed to this special issue in many ways. We hope the readers will enjoy this special issue, and look forward to your feedback and future contributions in this field.

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